REMARKS

Claims 1-7 are pending. Claim 1 is the only independent claim. No amendments have been made to the claims. A copy of the claims is provided above for the convenience of the Examiner. The specification has been amended to address the informality mentioned at page 2 of the Office Action. Withdrawal of the objection is requested.

Claims 1-6 were rejected under 35 U.S.C. § 103 over U.S. Patent 6,728,271 (Kawamura et al.) in view of U.S. Patent Publication No. 2004/0160898 (Lim et al.). Applicant traverses and submits that independent claim 1 is patentable over the cited art for at least the following reasons.

Claim 1 is directed to a packet processing circuit including: a plurality of macros each of which processes packet data on the basis of a clock and outputs the processed packet data from at least one route, the macros being cascade-connected; and a clock supply unit which supplies the clock to a macro to be controlled and, when no packet data is output for a predetermined time from all routes of a macro on an input side of the macro to be controlled, stops supplying the clock to the macro to be controlled.

In claim 1, the macros are connected in a cascade configuration, for example, like the configuration shown in Figure 1. A clock supply unit stops supplying a clock to a macro that can receive packet data from the output of another macro (i.e., a macro at the input side of the macro being controlled) when no packet data is output from all routes of the macro that is at the input side of the macro being controlled.

For example, referring to Figure 1, if no packet data is output from user block 1 (which is at the input side of user block 2) for a predetermined time, then the clock supply unit 5 will stop supplying the clock to the user block 2. This can also function to stop the clock supply to user block 3, for example when no packet data is output from user block 2 (which is at the input side of user block 3). Of course, the present invention is not limited to the disclosed embodiments.

While Kawamura et al. teaches the general concept of cutting off a clock signal to lower power consumption, it does not teach or suggest that power is cut off in the same manner as recited in claim 1. Kawamura et al. relates to a stream demultiplexing device. In Kawamura et al., plural transport packets are received, each of which contains a payload carrying a data portion from one of a multitude of elementary streams of data that have been multiplexed together.

In Kawamura et al., a payload processor extracts data from current transport packet and stores the extracted data into a data storage corresponding to the stream to which the data belongs. In Kawamura, power is cut off to the payload processing unit once this payload processing unit finishes storing the data for a particular transport packet. Power is resumed a predetermined time after the start of receipt of the next transport packet.

However, there is no teaching or suggestion in Kawamura of the clock supply unit that stops supplying a clock to a macro that can receive packet data from the output of another macro (at the input side of the macro being controlled) when no packet data is output from all routes of the macro that is at the input side of the macro being controlled. This is recognized in the Office Action. However, the position was taken in the Office Action that Lim remedies this deficiency. Applicant disagrees.

First, even if the references were to be combined, they would still not meet all the terms of claim 1. In Lim, power on for a module is performed when Ethernet handshaking signals indicate that a packet is arriving. Each module is provided with a logic circuit that monitors the handshaking signals provided to that module. If the handshaking signals indicate a packet is about to be transmitted to that module, power up of that module is performed.

Subsequent power down of the module is performed automatically when the entire packet has been transferred from the module. For example, as discussed at paragraph [0024], a logic circuit in the MAC-RX (Figure 1) controls that module to power down automatically when the entire packet has been transferred to the corresponding RX module. However, this power reduction method does not meet the above-mentioned limitation of claim 1 relating to the clock supply unit,

which supplies the clock to a macro to be controlled and, when no packet data is output for a predetermined time from all routes of a macro on an input side of the macro to be controlled, stops supplying the clock to the macro to be controlled.

The Office Action, at page 6, refers to paragraph [0031], which discusses an alternative embodiment in which modules "remain powered up even after they have finished transmitting any packet(s) within them." However, this portion also does not remedy the deficiencies of the portions of Kawamura and Lim discussed above. Even if modules are powered up a predetermined amount of time after they transmit a packet within them, this does not correspond to the recited feature of the clock supply unit. The clock supply unit of claim 1 controls application of a clock signal to a particular macro, not on the basis of whether that macro has transmitted a packet within it, but based on whether packet data has been output from ***a macro at an input side*** of the macro being controlled.

In fact, Lim teaches the module **powering *itself* down** based on what ***it has done*** with a packet within it, whether this is done immediately upon transmitting the packet (as in Lim's paragraph [0024]), or a predetermined time afterward (as in Lim's paragraph [0031]). On the other hand, claim 1 recites that the clock supply unit, which supplies the clock to a macro to be controlled, stops supplying the clock to the macro to be controlled *when no packet data is output for a predetermined time from all routes of a macro on an input side of the macro to be controlled.*

For at least the above reasons, even if the reference were to be combined, they would not meet the features of claim 1. For at least this reason, no prima facie case of obviousness has been set forth.

Moreover, there would have been no reason to combine the references so as to modify Kawamura et al. to use the technique taught in Lim. Lim relates to reducing power consumption in data switches by only turning on some modules when they are required to process data packets passing through the circuit. However, there would have been no reason to apply the power supply scheme of Lim into the demultiplexing device of Kawamura et al.

Kawamura et al. schedules the periods in which the clock is not supplied in accordance with the specific functional requirements particular to a demultiplexer. For example, the power is controlled based on activities and data receipt related to the demultiplexing function, such as when the data for the current transport packet has been safely stored in its appropriate storage location.

Substituting other power reduction techniques, such as those discussed in Lim, into the Kawamura system would change the principle of operation of Kawamura, and not take into account the reason Kawamura selects the time periods it does, i.e., in accordance with events occurring during the demultiplexing process. In fact, there would be no reason to modify Kawamura, which reduces power in accordance with the needs of a demultiplexing device, with other power reduction schemes, other than to meet the recited terms of the claim, which would be totally improper.

For at least the above reasons, independent claim 1 is believed patentable over the cited references, taken individually or in combination. The other claims are dependent upon claim 1 and are patentable for at least the same reasons.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

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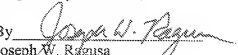
Respectfully submitted,

By 

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